REMARKS

Applicant respectfully requests reconsideration of this application as amended.

Office Action Rejections Summary

Claims 1 – 5, 7 – 14, 16 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,150,223 to Chern et al. (hereinafter "Chern") in view of U.S. Patent 5,976,991 to Laxman et al. (hereinafter "Laxman"). Claims 15, 18 and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chern and Laxman as applied to claims 11 and 17, and further in view of U.S. Patent 6,235,597 to Miles (hereinafter "Miles").

Status of Claims

Claims 1 – 5, 7 – 16, 18, and 19 remain pending in the application. Claims 1, 11, 15, and 18 have been amended. The amended claims are supported by the specification and drawing as filed and no new matter has been added. Claim 17 has been canceled. No new claims have been added. In light of the canceled claim, the following remarks relate to the pending claims.

Rejections Under 35. U.S.C. § 103(a)

Claims 1 – 5, 7 – 14, and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chern in view of Laxman. Applicant respectfully submits that claims 1 – 5, 7 – 14, and 16 are patentable over Chern and Laxman.

Amended independent claim 1 provides:

> A method of forming sidewall spacers adjacent opposing vertical sides of a gate electrode, comprising:
>
> forming at least one gate electrode over a substrate;
>
> forming, at a first temperature in a range of approximately 550°C to 580°C and a first pressure of about 10 mTorr, a first silicon oxide film

conformally over the substrate and gate electrode from a combination of gases including bis-(tertiarybutylamino)silane and oxygen;

forming, at a second temperature in a range of 580°C to less than 600°C and a second pressure of about 65 Pascal, a silicon nitride film conformally over the first silicon oxide film from a combination of gases including bis-(tertiarybutylamino)silane for about 49 minutes;

forming a second silicon oxide film over the silicon nitride film from a combination of gases including bis-(tertiarybutylamino)silane and oxygen; wherein the first temperature is less than the second temperature;

removing the second silicon oxide film to form an L-shaped spacer; and

implanting a dopant through the L-shaped spacer to form a region of intermediate dopant concentration and depth between a tip region and a source/drain region. (emphasis added)

Amended independent claim 11 provides:

A method of forming a transistor, comprising:

forming at least one gate electrode over a gate dielectric layer, the gate dielectric layer disposed on a substrate;

depositing a first silicon oxide film conformally over the substrate and gate electrode from a combination of gases comprising bis-(tertiarybutylamino)silane and oxygen at a first temperature of between approximately 550°C and 580°C and a pressure of about 10 mTorr;

depositing a silicon nitride film conformally over the first silicon oxide film from a combination of gases comprising bis-(tertiarybutylamino)silane and ammonia at a second temperature of between 580°C and less than 600°C and a second pressure of about 65 Pascal for about 49 minutes;

depositing a second silicon oxide film over the silicon nitride film from a combination of gases comprising bis-(tertiarybutylamino)silane and oxygen;

forming a first sidewall spacer; wherein the first temperature is less than the second temperature;

removing the second silicon oxide film to form an L-shaped spacer; and

implanting a dopant through the L-shaped spacer to form a region of intermediate dopant concentration and depth between a tip region and a deep source/drain region. (emphasis added)

Chern discloses a method for forming a double-layer spacer. In particular, Chern discloses, "A standard self-aligned reactive ion etch is applied to form contact vias, such as bit-line to the substrate 34A of the interior circuit, the bit-line to gate 34B, and the bit-line to

the substrate 34C of the peripheral circuit in the embodiment, in third silicon oxide layer by anisotropical etching" (col. 3, lines 15 – 20, and Figure 7). Nothing in Chern discloses or suggests implanting a dopant to form a region of intermediate dopant concentration and depth between a tip region and a deep source/drain region. In fact, nothing in Chern discloses implanting dopants into the substrate.

Laxman discloses a method to form silicon oxynitride films. The method disclosed by Laxman is limited to various films for semiconductor devices. Nothing in Laxman discloses or suggests implanting a dopant to form a region of intermediate dopant concentration and depth between a tip region and a deep source/drain region. As such, Laxman fails to cure the deficiency of Chern.

Applicant respectfully submits that there is no motivation to combine Chern and Laxman, as nothing in Lax suggests implanting a dopant to form semiconductor devices. As such, applicant respectfully submits that Chern would not be motivated to look at Laxman to form a region of intermediate dopant concentration and depth between a tip region and a deep source/drain region.

Even if Chern and Laxman were somehow combined, the combination would still not include all the limitations of independent claims 1 or 11. In particular, claim 1 includes the limitation of "implanting a dopant through the L-shaped spacer to form a region of intermediate dopant concentration and depth between a tip region and a source/drain region." The combination of Chern and Laxman does not teach this limitation. As disclosed in the application as filed, the spacer of the present invention provides an improved and more gradual doping profile, which results in the series resistance from the tip in to the source/drain region being reduced (page 7, lines 8 – 13). As such, applicant respectfully submits that claims 1 and 11 are patentable over the combination of Chern and Laxman under 35 U.S.C. §103(a) and request removal of the rejection.

Claims 2 – 5 and 7 – 10 each depend either directly or indirectly from independent claim 1, and thus include the limitation of "implanting a dopant through the L-shaped spacer to form a region of intermediate dopant concentration and depth between a tip region and a source/drain region." Claims 12 – 14, and 16 each depend either directly or indirectly from independent claim 11 and include the limitation of "implanting a dopant through the L-shaped spacer to form a region of intermediate dopant concentration and depth between a tip region and a source/drain region." As such, applicant respectfully submits that dependent claims 2 – 5, 7 – 10, 12 – 14, and 16 are also patentable over the combination of Chern and Laxman, and request removal of the rejection under 35 U.S.C. §103(a).

Claims 15, 18 and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chern and Laxman and further in view of Miles. Applicant respectfully submits that claims 15, 18, and 19 are patentable over Chern, Laxman, and Miles. Claims 15, 18, and 19 each depend either directly or indirectly from independent claim 11 and thus include the limitation of "implanting a dopant through the L-shaped spacer to form a region of intermediate dopant concentration and depth between a tip region and a source/drain region." As discussed above, nothing in Chern or Laxman discloses this limitation.

Miles discloses a semiconductor structure having gates formed on a substrate. In particular, Miles discloses, "If desired, dopants 10 can optionally be implanted into the substrate in the spacing between adjacent gates. Typical dopants include n-type dopants such as phosphorous and arsenic and p-type dopants such as boron. The dosage of the dopants is typically about 1E12 to about 1E15" (col. 3, lines 1 – 5, and Figure 1). In particular to ion implantation, the Office Action states, "Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form source/drain regions adjacent to the gate of Chern as taught by Miles to reduce source/drain depth adjacent to the gate" (06/24/2005 Office Action, page 8, lines 5 – 9). Applicant respectfully

submits that othing in Miles discloses implanting a dopant to form a region of intermediate dopant concentration and depth between a tip region and a deep source/drain region. In fact, all the figures in Miles only show a consistent amount of dopant within the substrate. As such, Miles fails to cure the deficiencies of Chern and Laxman. Moreover, applicant respectfully submits that because the combination of Chern, Laxman, and Miles do not include all the limitations of claim 11, dependent claims 15, 18, and 19 are patentable over the combination under 35 U.S.C. §103(a) and request removal of the rejection

In conclusion, applicant respectfully submits that in view of the arguments set forth herein, the applicable rejections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Suk Lee at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,
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Judy L. Steinkraus 08/24/2005

Application No.: 09/752,798 **Filing Date:** 12/28/2000 **Docket No.:** 42390.P8119
Date Mailed: 08/24/2005 **Due Date:** 08/24/2005 **Atty/Sec:** MAB SSL jxs
Client: Intel Corporation
Title: METHOD OF MAKING SIDEWALL SPACERS USING BTBAS
First Named Inventor: Mohamad Arafa

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